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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): CYPR-CD00232

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on 10/09/07

Signature Donna Petford

Typed or printed name DONNA PETFORD

Application Number	Filed
10/033,027	10/22/01

First Named Inventor: SNYDER

Art Unit	Examiner
2183	PAN, D.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☒ attorney or agent of record. Registration number 35,295
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Signature

ANTHONY C. MURABITO
Typed or printed name

(408) 938-9061
Telephone number

10/09/07
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Snyder

Serial:	10/033,027	Group Art Unit: 2183
Filed:	10/22/2001	Examiner: Daniel H. Pan
For:	PROGRAMMABLE MICROCONTROLLER ARCHITECTURE	

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and
EXAMINER INTERVIEW SUMMARY

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Alexandria, VA 22313-1450

Dear Sir:

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Appellants respectfully assert that there is no motivation to combine Tzori in view of Insenser, as proposed by the rejection. Therefore, the cited combination does not render obvious the claims. The rejection proposes the modification in order to "includ(e) the analog blocks as claimed." Herein, the rejection concedes that the rejection was improperly guided by hindsight in view of the claims of the present application.

Moreover, Tzori is directed to a system for simulation/emulation of digital logic (Title, Abstract, *inter alia*, emphasis added). Appellants respectfully assert that one of ordinary skill in the art would not be motivated to improve simulation/emulation of digital logic by the addition of analog function blocks, as proposed by the rejection.

Per *In re Vaeck,* 947 F.2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991), "[a] proper analysis under § 103 requires, *inter alia*, consideration of... whether the prior art would have suggested to those of ordinary skill in the art that they should make the claimed composition or device, or carry out the claimed process." Regardless of the type of disclosure, the prior art must provide some motivation or suggestion to one of ordinary skill in the art to make the claimed invention in order to support a conclusion of obviousness.

As there is no suggestion in the art to make the proposed modification, Appellants respectfully assert that the rejection relies upon impermissible hindsight to forge a combination of disparate references guided only by the disclosure and claims of the present application. Consequently, the rejection fails to establish *prima facie* obviousness.

Further, the proposed addition of analog blocks clearly changes the digital principle of operation of the primary reference. Per *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959), "if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." As the proposed modification changes the principle of operation of the primary reference, the rejection fails to establish *prima facie* obviousness.

The rejection relies upon numerous unjustifiable interpretations of the cited art. For example, the rejection alleges an "IC socket is an integrated circuit." Appellants traverse. As is

known, an IC socket is a mechanical device that may accept, remove or replace an IC. Without a mated IC, the IC socket has no logic or analog function.

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The rejection alleges that Tzori "pod 32" suggests the claimed bus and recited couplings of said bus. Appellants traverse. As understood by Appellants, "pod 32" is a printed circuit board assembly comprising at least six integrated circuits and other components, including a socket for another IC, as described above and in Figure 1. Appellants respectfully assert that one of ordinary skill in the art would not understand "pod 32" as the recited "bus."

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The rejection alleges that "circuit board trace 42... (is) dynamically configurable and programmable." Appellants traverse. Tzori teaches "[a]ll IC pin-receptacles 38 included in the IC socket 34 connect by individual printed circuit board traces 42 to the configurable-logic IC 36a or 36b" (column 8, lines 30-33). Thus, Tzori teaches traces 42 are static and non changing, connecting pins of the IC socket to other ICs. As the rejection's interpretation of the cited art is demonstrably incorrect, the alleged teachings are not present, do not suggest the claimed limitations, and the rejection fails to establish *prima facie* obviousness.

The rejection alleges that Tzori teaches the Claim 1 limitation of configuration "with a single register write operation." Appellants traverse. Tzori teaches sending configuration data in a serial manner (column 9 line 9-30). This passage, as well as the whole of Tzori, fails to teach

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Appellants respectfully assert that van der Wal is non-analogous art per *In re Clay*, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992). Per *In re Clay*, a reference must "(commend) itself to an inventor's attention in considering his problem." Appellants respectfully assert that van der Wal is directed to a "real time modular video processing system" (Abstract). Appellants do not find the video processing systems taught by van der Wal to commend van der Wal to Appellants in consideration of Appellants' problem. For example, the claims of the present invention are not directed to video processing.

Appellants respectfully assert that van der Wal would not commend itself to one of ordinary skill in the art in consideration of the problems solved by the present invention, due to the myriad well known differences between video processing systems and configurable microcontrollers, as disclosed and claimed in the present application. Appellants respectfully assert that the citation of van der Wal is improper, and that all rejections dependent upon van der Wal are therefore overcome.

In summary, Appellants respectfully submit that the Examiner's rejections of the Claims are improper as key limitations needed for proper *prima facie* rejections of Appellants' Claims are not met by the cited references as outlined above. Key limitations of independent Claims 1, 11, 17, 35, 37, 42, 51, 52 and 58 (from which Claims 2-10, 13-16, 18, 20, 21, 23-34, 36, 38-41, 43-49, 57 and 59 depend) are not taught or suggested by the cited art. In addition, the proposed combinations of art are improper, as outlined above. Appellants respectfully submit that the rejections of Claims 1-11, 12-18, 20-21, 23-49, 51-52 and 57-59 are improper and should be reversed.

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MURABITO, HAO & BARNES LLP

Date: oct 9, 2007

Anthony C. Murabito
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